Annual Technical Report

Materials Processing and Device Development to Achieve Integration of Low Defect Density III Nitride Based Radio Frequency

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The principal goal of the ongoing program is the enhancement of the functionality of silicon by expanding its field of use to include a higher frequency of operation via the integration of silicon-based IC circuits and GaN-based HFETs to produce variable gain amplifiers as the proof of concept of an electronic microsystem. This will be demonstrated by on-chip digital control of the gain of the GaN HFET device using a CMOS gate circuit. During this reporting period, NCSU and Nitronex have completed the construction and commissioning of two proprietary 100mm III-Nitride MOVPE systems, developed a process route for the growth of GaN on Si(111), demonstrated growth of GaN on 50-mm and 100-mm diameter Si(111) substrates, and transferred in-house pendeo-epitaxy techniques developed from NCSU to Nitronex. Also during this reporting period, GTRI developed a wafer processing procedure, validated each process step and fabricated working devices on sapphire substrates. Transconductance of these devices is approximately 140 mS/mm and the saturated drain to source current at zero gate bias is 700m A/mm.

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Nitronex Corporation
Annual Technical Report

Heterogeneous Materials and Systems Integration via Selective Growth of Gallium Nitride-based RF components and Silicon Integrated Circuits

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Prepared for

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1.0 Summary

The principal goal of the ongoing program is the enhancement of the functionality of silicon by expanding its field of use to include a higher frequency of operation via the integration of silicon-based IC circuits and GaN-based HFETs to produce variable gain amplifiers as the proof of concept of a electronic microsystem. This will be demonstrated by on-chip digital control of the gain of the GaN HFET device using a CMOS gate circuit.

The platform chosen for this initial integration demonstration will be a 100-mm Si(001) substrate that is fully CMOS compatible. The materials stack will be comprised of the following: AlGaN/GaN HFET device material stack, Pendeo-epitaxially grown GaN buffer, an AlN buffer, and a Si(111)/Si (100) SOI wafer with micromachined structures for thermal management.

Nitronex's primary role in this interdisciplinary collaborative research program is the materials integration of heteroepitaxially grown GaN-based epilayers (using a MOVPE deposition technique) with large-area (100mm) silicon (100) wafers. During the past year Nitronex has completed construction and commissioning of a proprietary 100mm III-Nitride MOVPE system specifically designed to address the uniformity issues required for commercial applications, has developed a process route for the growth of GaN on Si(111), has demonstrated growth of GaN on 50-mm and 100-mm diameter Si(111) substrates, and has transferred to in-house the Pendeo-epitaxy technique developed at NCSU.

2.0 Large Diameter MOVPE Equipment

In developing a reactor for large-diameter epitaxial growth of the III-Nitrides, the most important parameters in obtaining uniform high quality deposition are those related to the gas injection and the uniformity of substrate heating. *These requirements are further exacerbated in the development of the PENDEO™ process, as this lateral growth technique is highly dependent on uniform flow and temperature profiles.* By meeting our own internal uniformity specifications requisite of the pendeo-epitaxial growth technique, we our confident that will be able to achieve 5% uniformity in thickness, composition and doping across the 100-mm wafers.

Wafer carriers are typically heated either by radio frequency (RF) induction or by resistive heating elements. RF heating has the advantage of minimizing the contact between the heating mechanism and process gases. However, uniform heating of large areas by induction is difficult and inefficient. Nitronex's MOVPE system is a vertical reactor with resistive heating capable of deposition on three 50-mm wafers (3 x 2") or a single 100-mm wafer (1 x 4"). The design of this reactor will provide a platform for testing improvements in reactor design that will lead to a reactor for multiple 100-mm wafers (i.e. 3 x 4"). A technical description of Nitronex's vertical reactor design is outlined in the following paragraphs.

2.0.1 *MOVPE System Overview*

The Nitronex 100-mm System (Figure 1) consists of a gas delivery cabinet, reactor chamber cabinet and electronics cabinet. The gas delivery cabinet houses state-of-the-art

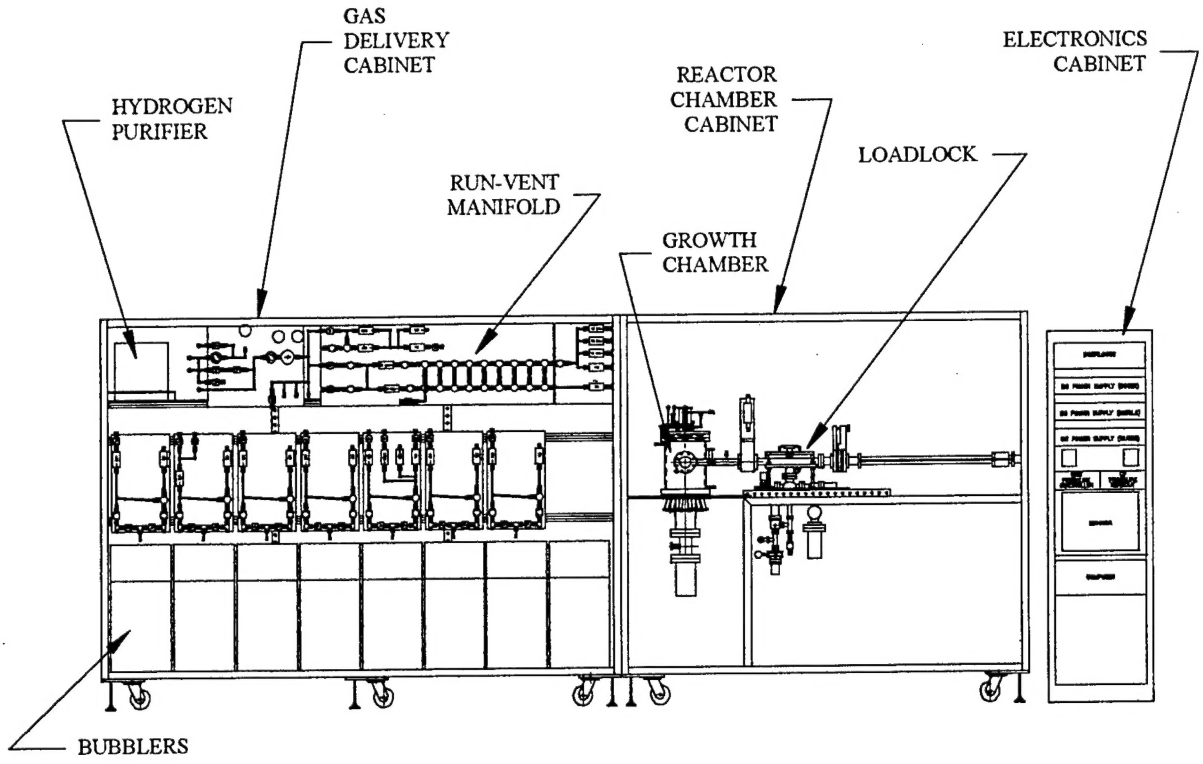


Figure 1. Nitronex MOCVD System Schematic.

purifiers (hydrogen, nitrogen and ammonia), the run-vent manifold and seven alkyl bubblers. The reduced deep volume run-vent manifold is located near to the reactor chamber to minimize the gas line length to the reactor chamber. This design reduces sweep time and contributes to sharper interfaces for multi-layer depositions, especially multiple quantum well structures. The reaction chamber cabinet contains the growth chamber, process pump and load lock. The growth chamber is water-cooled and contains a heated substrate mount (1200°C) with three independently controlled zones, as well as a 1500-rpm substrate rotation capability. The growth chamber is connected to the load lock by a rectangular gate valve. The substrate carrier is transferred between the growth chamber and load lock by a magnetically coupled linear transfer device. The electronics cabinet houses the power supplies, system interlocks and computer control system. The components in all three cabinets have been arranged to allow for ease of maintenance and modification. The most unique aspects involve the multi-zone systems for gas injection and substrate heating.

2.0.2 *Gas Injection*

Having control of the radial concentration of the injected gases is key to obtaining uniform large area deposition. The radial concentration can be controlled by adjusting the geometry of the injection nozzle. However, since multiple injection nozzle geometries must be tried, the fabrication and testing necessary to find the optimum configuration would be time

consuming and expensive. Furthermore, the optimum geometry may be different for different operating temperatures, flows and pressures. We have chosen to use a proprietary design comprised of multiple concentric injection zones (metal-organic alternating with ammonia) with input for each zone controlled by a separate mass flow controller. Such an arrangement allows for precise control of the radial concentration of the process gases during film growth. The use of a curtain gas helps to minimize wall deposition while maintaining uniform flow across the chamber. In addition, the use of the metal-organics and ammonia is more efficient since they are input only across the diameter of the wafer carrier.

2.0.3 *In-Situ Capabilities*

The proprietary gas injector is designed with two optic ports for *in-situ* film deposition analysis. These ports are designed at an incident angle normal to the growth surface to facilitate using interferometry for film thickness measurements and using optical fiber infrared thermometry for substrate temperature measurements.

The commercially available interferometry monitoring system uses spectral reflectance to measure deposition rates, layer thickness, optical constants and uniformity. An integrated silicon photodiode allows for continuous *in-situ* monitoring even at elevated rotation speeds (i.e. 1500 rpm) in either the 1 x 4" or 3 x 2" system configurations. This *in-situ* monitoring tool coupled with our computer control system, described below, will allow for real-time analysis of the growth process.

2.0.4 *Multi-Zone Substrate Heater*

The Nitronex reactor uses a multi-zone resistance heater to insure temperature uniformity across the wafer carrier. With a single zone heater, lower temperatures usually occur near the edge and center support of the wafer carrier. The lower temperatures at the edge are due to the increased gas flow in this region as well as heat loss to the water-cooled reactor wall. Additionally, the center support for the wafer carrier can act as a heat sink leading to reduced temperatures at the center of the carrier. We reduce the heat loss through the center support using a proprietary design to minimize the cross section of the support.

Tungsten and graphite are materials that are commonly used for resistive heating elements. However, both of these materials degrade and become embrittled when exposed to the process gases used in the deposition of GaN. The Nitronex system uses elements made of rhenium, a high temperature refractory metal well suited for use in hydrogen and ammonia environments.

2.0.5 *Computer Control*

The Nitronex 100-mm MOCVD system is fully computer controlled and automated. The in-house designed control software is robust and user-friendly. It can be run in manual mode, automatic (recipe) mode or recipe control with manual override. Recipe control is a must for repeatable process control. Additionally, process and system parameters are stored in a database to facilitate detailed analysis of the process. The backplane of the computer-controlled system is oversized to allow for the implementation of additional mass flow controllers and pneumatically actuated valves should subsequent system modification become necessary.

The optical fiber infrared pyrometer and multi-zone substrate heater power supplies are close-loop controlled. Additional thermocouples are used in balancing the power requirements between the heating zones to insure temperature uniformity across the wafer carrier. With the closed-loop temperature control, in-situ film monitoring system and data acquisition capabilities, Nitronex has the ability to provide real-time process control for nitride growth.

3.0 GaN growth on 50-mm Si(111)

Nitronex has demonstrated the basic steps necessary for single-crystal deposition of 2H-GaN on Si(111). This has been achieved by incorporating the use of a transition layer comprised of a thin 3C-SiC carbonization layer and an aluminum nitride (AlN) buffer layer. Figure 2 is a Scanning Electron Microscopy (SEM) image, performed at NCSU, showing the cross-section of a typical GaN/AlN/3C(SiC(111)/Si(111) materials stack.

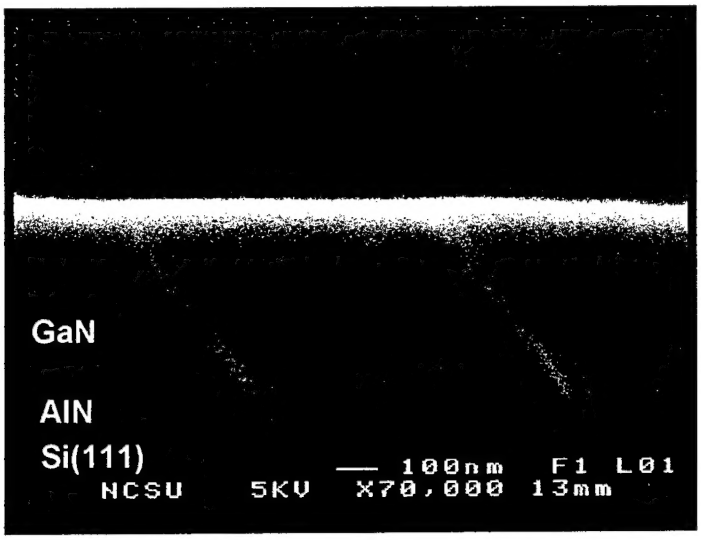


Figure 2. Cross-sectional SEM of GaN/AlN/Si(111) material stack.

Over the last few months, the Nitronex team has continued to refine and optimize the formation of the transition structure. By doing so, we have been able to improve the quality of our GaN epilayers. This is evident by the improvement of our initial GaN layers grown on the AlN/3C-SiC/Si(111) exhibiting typical XRD FWHM values of ~ 1000 arcseconds. Our most recent GaN layers now exhibit typical XRD FWHM values of ~500 arcseconds, indicative of an improved crystal structure. Recent low-temperature (14 K) photoluminescence spectra of these films are comparable to similar GaN layers grown on 6H-SiC as shown in Figure 3.

Nitronex is aggressive pursuing further refinements in the transition layer scheme to further improve the quality of our GaN epilayers and reduce the cracking resulting from the mismatch in coefficients of thermal expansion.

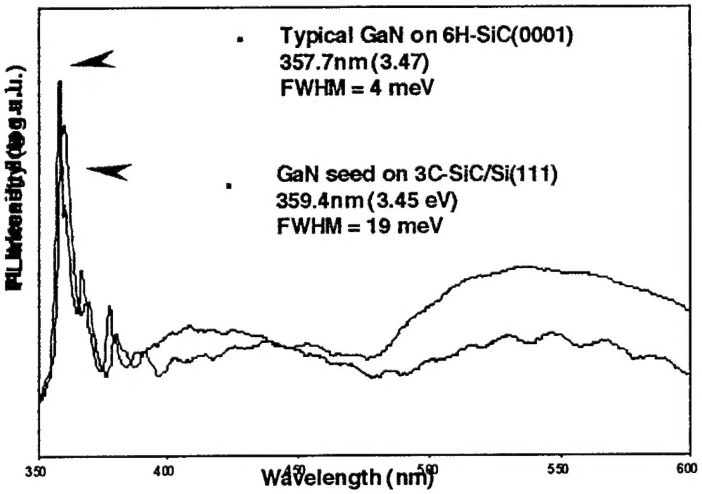


Figure 3. Low-temperature PL spectra of 1μm thick GaN(0001) films grown on AlN/6H-SiC(0001) and AlN/3C-SiC/Si(111).

The GaN epilayer thickness uniformity has been characterized using a Filmetrics F50 spectrometer thin-film mapping system. The variations across the 50-mm samples were measured to be 17.1%, as shown below in Figure 4.

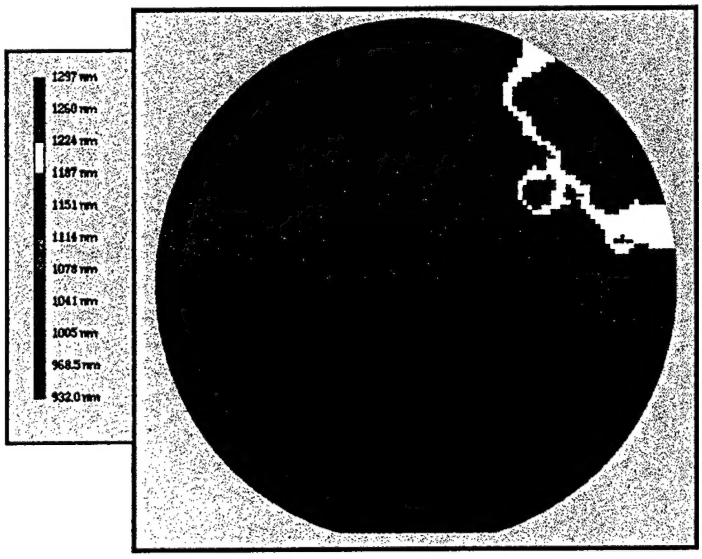
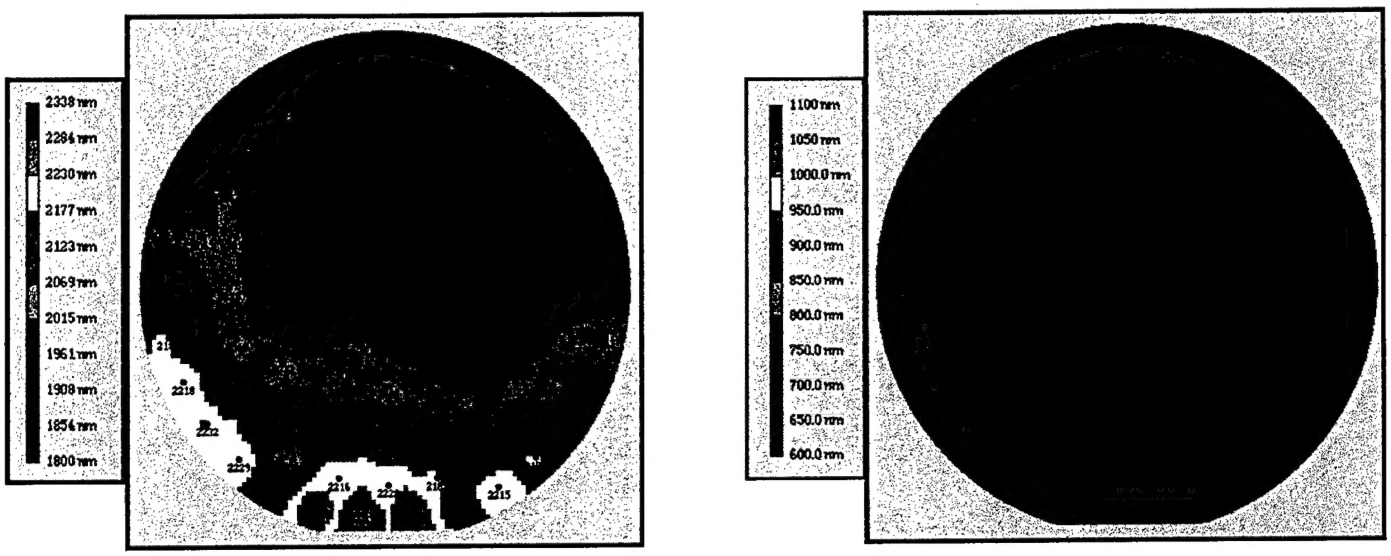


Figure 4. Thickness uniformity of a typical GaN epilayer on 50-mm Si(111).

4.0 Scale-up to 100-mm Si(111)

Nitronex, using the facilities at the NCSU Davis Research Labs, achieved initial growth of GaN on 100-mm Si(111) in the Spring of 2000. This process was successfully transferred in-house to Nitronex in July 2000 with improved thickness uniformity across the 100-mm wafers, as shown in Figure 5.



a) NCSU prototype III-Nitride MOVPE
Uniformity ±30.7%

b) Nitronex Custom III-Nitride MOVPE
Uniformity ±10.3%

Figure 5. Thickness uniformity of initial GaN epilayers grown on 100-mm Si(111).

5.0 Future Plans

The long term focus of Nitronex's research and development strategy is the materials integration of device quality GaN with Si(001). A GaN/Si integration scheme requires the use of Si(111) substrates for GaN growth and Si(001) substrates for eventual CMOS fabrication. One method to achieve the desired substrate is to utilize a Si (111)/Si (001) wafer, which is a variation of commercially available SOI wafers. Nitronex will use this SOI platform to grown 100-mm GaN.

The optimization of the PENDEO™ process and the scale-up to a 100-mm platform are another focus for the coming year. Control of the lateral growth morphology, elimination of the defects associated with coalescence and reduction of the epilayer crack density are all goals for the growth of high quality pendeo-epitaxial GaN. We believe that the PENDEO™ process is superior to the competing LEO growth techniques in that the need for a growth mask and the consequential crystallographic tilt are eliminated. Preliminary studies regarding pendeo-epitaxial growth show no evidence of crystallographic tilt and no mis-registry at points of coalescence.

Scale-up to 100-mm will require the stringent uniformity requirements in gas flow and temperature that have been addressed in the Nitronex 100-mm MOVPE system design. However, this uniformity is also influenced by the total gas flow, the gas consumption, chamber pressure, rotation rate, and diluent gas consumption. Moreover, the processing parameters and sequence also play a role on the final quality of the pendeo-epitaxial grown thin films. Of particular interest are the selections of the seed post and separation widths. The influence of the growth parameters as well as the processing parameters on the wafer scale demonstration of pendeo-epitaxial GaN will be examined with the two-fold goal of optimizing growth on existing 50-mm wafers and establishing guidelines for the 100-mm wafer growth of PENDEO™ GaN.

Additionally, there are two advanced approaches, namely S^2 and 1*Step* PENDEO™, that Nitronex will pursue to further advance the pendeo-epitaxial growth of GaN on silicon platforms. These techniques specifically address the susceptibility of large-area thin films under tensile stress to crack, thereby limiting their viability as device layers. Achievement of our stated goal "to engineer a wafer capable of withstanding the tendency to bow" may come at the expense of crack formation in the GaN epilayers. Thus further *growth* engineering and processes need to be considered.

Finally, Nitronex will grow material stacks for GaN-based heterojunction field effect transistors on silicon wafers. These test device layers will be delivered to Georgia Tech Research Center for evaluation and device demonstration. The goal is to use feedback from these test structures to help refine and optimize the multilayer growth techniques required for device fabrication.

Georgia Tech Research Institute

Project A6043 Annual Technical Report

Support of Heterogeneous Integration of GaN on Silicon

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Table of Contents

1.0 Summary 1

2.0 Process Steps 2

3.0 Ohmic Contact Measurements 6

4.0 Si MOS Fabrication 8

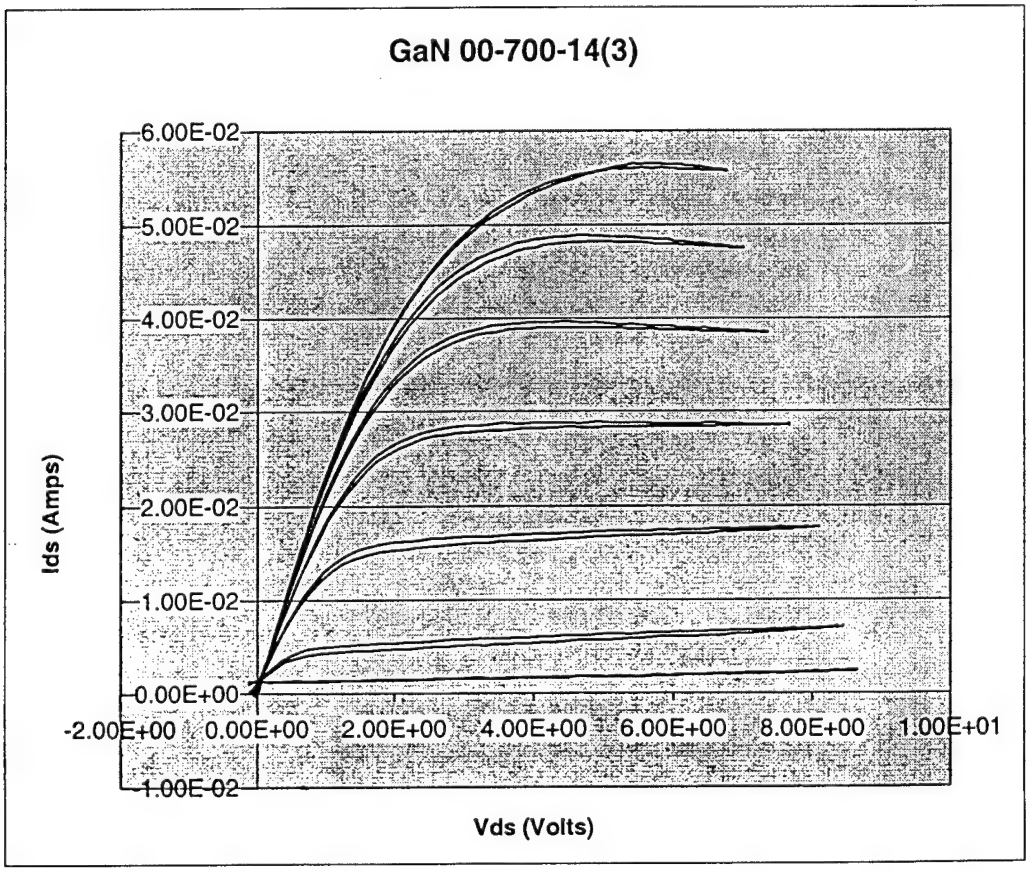
5.0 Integrated Circuit Fabrication 10

6.0 References 18

1.0 Summary

GTRI is assisting NCSU and Nitronex in a new heterogeneous materials technology that combines high performance RF gallium nitride devices and workhorse silicon MOS analog and digital devices on a low cost silicon substrate. The approach combines the advantages of both hybrid and monolithic technologies. Microwave transistors (GaN FETs) are integrated onto specially prepared silicon host wafers. These wafers are tailored to accept CMOS processing and interconnection to the GaN RF devices. Air bridge technology and thin film techniques are then used to provide the necessary interconnections.

During this reporting period, GTRI developed a wafer processing procedure, validated each process step and fabricated working devices on sapphire substrates. Transconductance of these devices is approximately 140 mS/mm and the saturated drain to source current at zero gate bias is 700 mA/mm. Figure 1 shows the IV characteristics of a typical device. The gate voltage step is 1V. GTRI also designed a new device mask set that permits on-wafer probing.



2.0 Process Steps

Figure 2 is a flow chart of the steps used in fabricating GaN GaN HFETs on SiC and sapphire substrates. The first step is device isolation. After patterning the wafer, a silicon tetrachloride-based reactive ion etch (RIE) process is used to form mesa structures as shown in Figure 3. Reproducible etch rates of 25 nm/min have been demonstrated using a power level of 200W on our Plasma Therm RIE system.

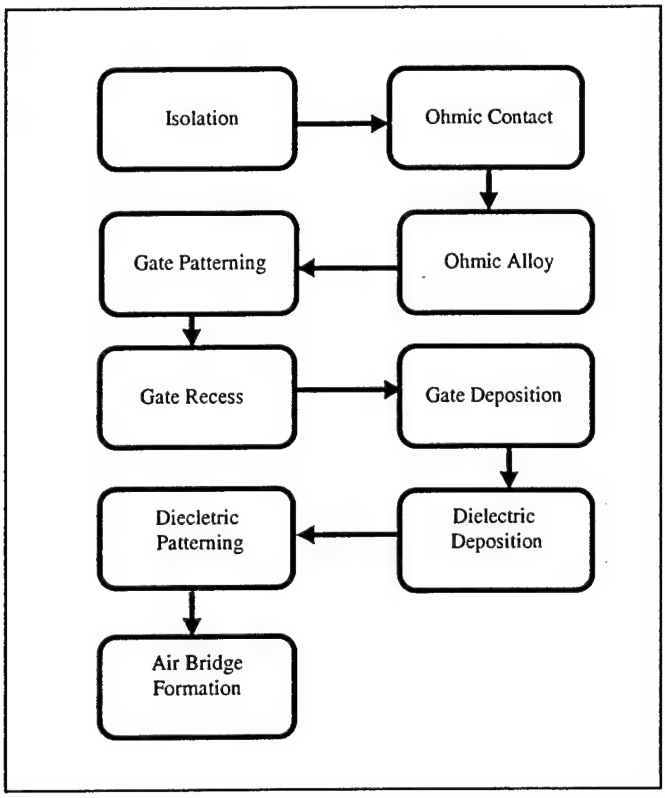


Figure 2. FET Process Flow Diagram.

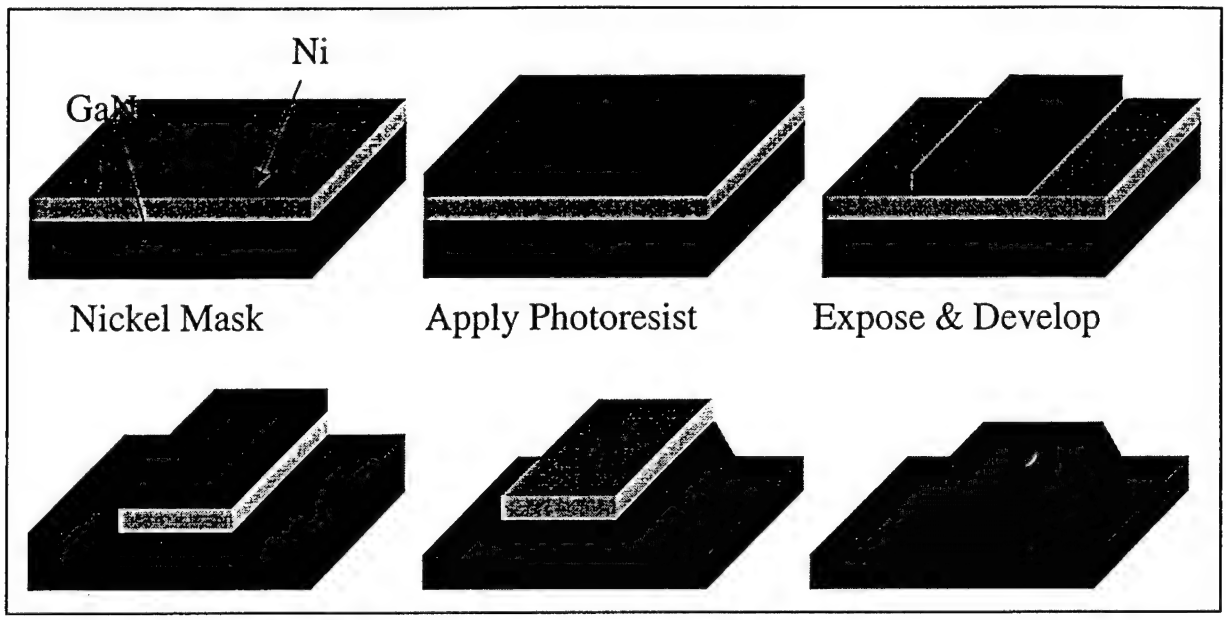


Figure 3. Mesa Isolation Process Steps.

Ohmic contacts, to the wide bandgap semiconductor, are second only to materials growth as a challenge to the realization of GaN-based HFET devices. Figure 4 shows the steps involved in fabricating ohmic contacts on GaN. We are currently using a metal system composed of titanium-aluminum-nickel-gold as shown in Figure 5. Rapid thermal annealing (RTA) at 900C for 30 sec. is used to alloy the contact metal to the semiconductor. Measurements on transmission line method (TLM) evaluation structures, fabricated as a part of our process control monitor (PCM), indicate that we are obtaining contact resistances of 1.3×10^{-6} ohm-cm^2, which is state of the art.[1]

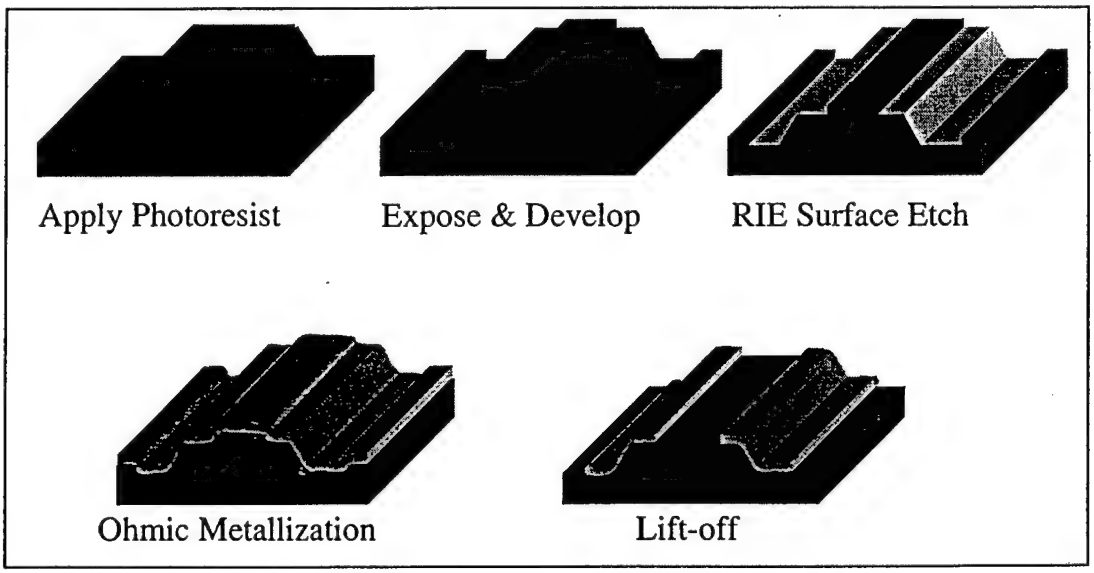


Figure 4 Ohmic Contact Process.

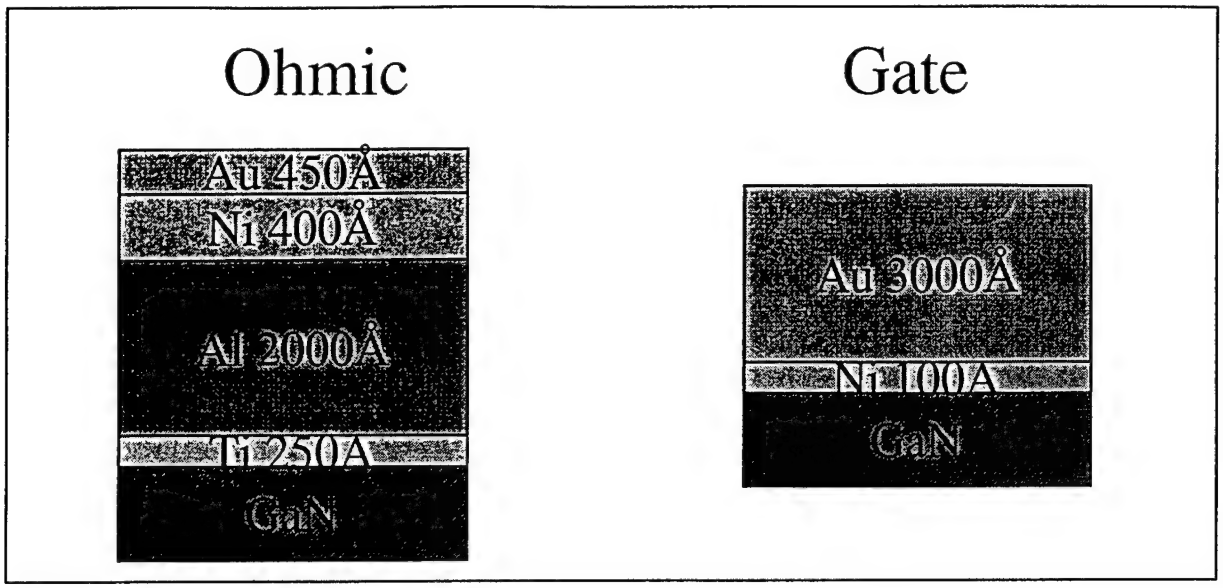


Figure 5 Ohmic and Schottky Gate Metallization Schemes.

Figure 5 also shows the metallization scheme that Georgia Tech is using to fabricate the Schottky barrier gate. This process is straightforward on GaN HFETs fabricated on SiC substrates; however, the defect density of the GaN material on silicon will strongly influence the quality of the Schottky diode. Georgia Tech will have a complete PCM chip having a number of test structures to fully evaluate the process.

Figure 6 is a photograph of a one-micron gate length GaN HFET fabricated on a SiC substrate using the process procedures described above. Drain to source spacing of this device is 3.5 microns and on-wafer probing can be used to measure performance.

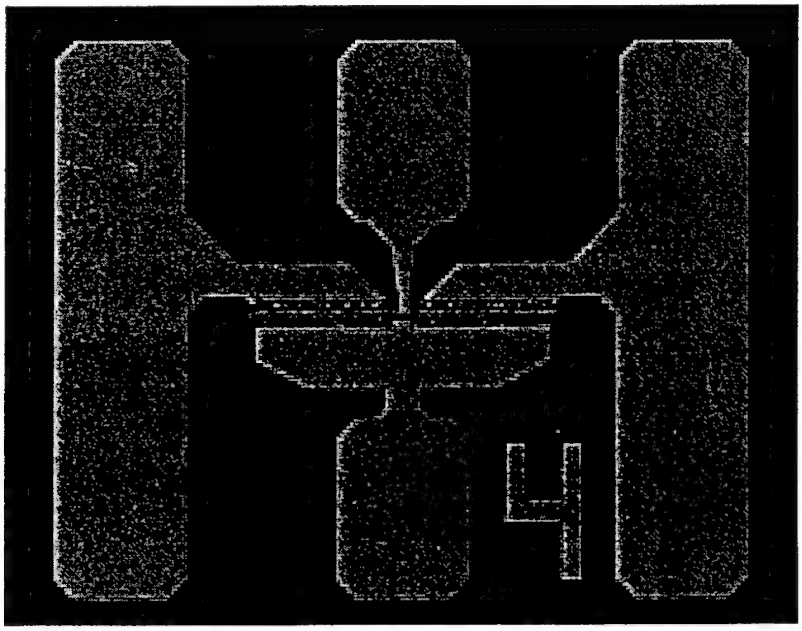


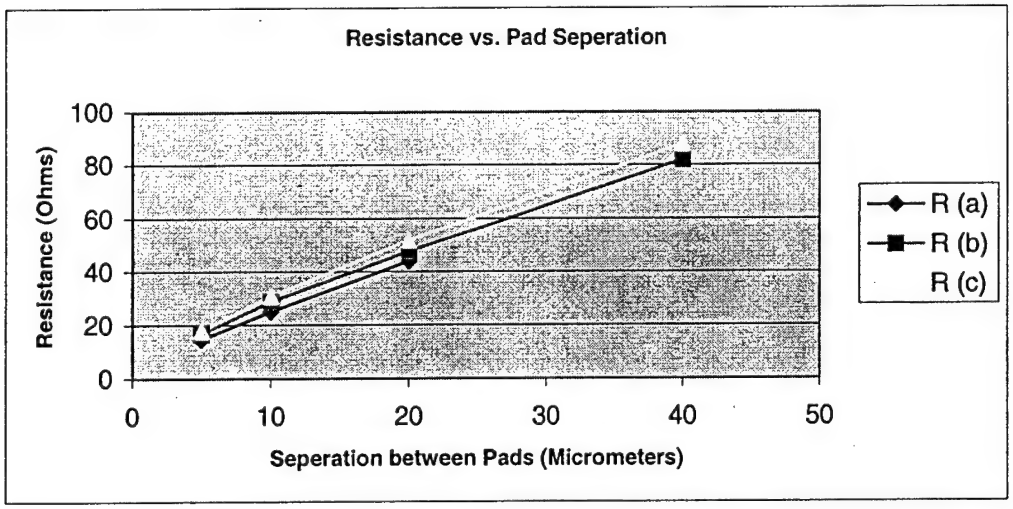
Figure 6. GaN HFET Fabricated on SiC Substrate.

On the basis of these results, our team will start with our baseline GaN process to demonstrate GaN HFETs on the mixed material system described above. We have analyzed the process chemistries and found that the GaN steps should not affect the silicon substrate. The only major concerns are the mechanical integrity of films and the thermal integrity of the layer structures of the integrated process. **Successful completion of this task represents a revolutionary breakthrough for low cost high power microwave devices and positions us to take the next step of demonstrating the heterogeneous integration of digital and analog microwave devices.**

3.0 Ohmic Contact Measurements

Using a test wafer, GTRI has demonstrated the ability to fabricate ohmic contacts for HFET devices on GaN. The test wafer consisted of a GaN thin layer grown on SiC with unknown doping concentrations.

The GaN ohmic test structure design contains diagnostic devices including ohmic resistance test structures. These structures consist of five aligned pads separated by distances of 5, 10, 20, and 40 microns respectively. The pads were constructed by overlapping squares of mesa, ohmic metal, and gate metal. Ohmic measurements were taken using a four-probe procedure. A current of 1 mA was forced from one pad to an adjacent pad while measuring the voltage change across the pad separation. Resistances were calculated with Ohm's Law and plotted against the respective separations (Table 1).



Distance	R (a)	R (b)	R (c)
5	14.7	16.9	17.9
10	25.1	28.9	30.8
20	43.9	47.7	51.9
40		81.9	87.8

Table 1. Resistance vs. Pad Separation.

The contact resistance, R_C, was calculated for each pair of pads (a). An average value of R_C was determined and used to find the contact resistance in units of ohm-mm (b) and ohm-cm^2 (c). Corresponding equations are given in Figure 7.

(a) $$R_C = \left| \frac{R_{ij}l_{jk} - R_{jk}l_{ij}}{2(l_{ij} - l_{jk})} \right| \text{ [ohm]}$$

ij refers to distance between pad i and pad j
jk refers to distance between pad j and pad k

(b) $r_C = R_C W$ [ohm-mm]

W refers to pad width in mm

(c) $r_C = R_C(W \times L_t)$ [ohm-cm^2]

W refers to pad width in cm
L_t refers to transfer length in cm.

Figure 7. Equations used to determine contact resistances.

Pad width was determined to be 0.1mm or .01 cm. The transfer length is the lateral length in the ohmic contacts that current flow is expected to cross. This value L_t was estimated at a typical value of 3.0×10^{-5} cm. Using these values and equations, the contact resistance was found in the following forms (Figure 8).

R_C(avg.) = 4.36 ohms

r_C = 0.436 ohm-mm

$r_C = 1.3 \times 10^{-6}$ ohm-cm^2

Figure 8. Contact resistance determination.

These findings demonstrate GTRI's ability to successfully test the resistance of ohmic contacts fabricated on GaN. However, the doping level of the wafer needs to be known for proper comparison and analysis of the devices.

4.0 Si MOS Fabrication

MiRC has established and maintains a baseline silicon CMOS process to provide a "platform" for research on a variety of new materials and device structures. The processing line is capable of 4"-6" wafer production. Devices such as CHEMFET sensing arrays and single-poly, single-metal CMOS circuits with 2-micron features have been successfully processed through the line. More complicated CMOS processes, including multilevel interconnection and 1-micron features, are in progress and will be completed by the end of this year. Upon the completion of the second baseline process, MiRC will be in the position to provide more flexibility in device design and layout. We expect to need this advanced process to support the heterogeneous materials program.

Along with the regular CMOS run, many processing steps designed for micron feature applications have been established and optimized. Especially, the steps such as RCA wafer cleaning, wet and dry oxidation, high temperature nitride growth, low-pressure polysilicon growth, low temperature oxidation, wet and dry etching, mask design and layout, sub-micron lithography, metallization, etc. have been standardized and serving the research community. Figure 9 shows a schematic of a CMOS inverter and its realization in silicon.

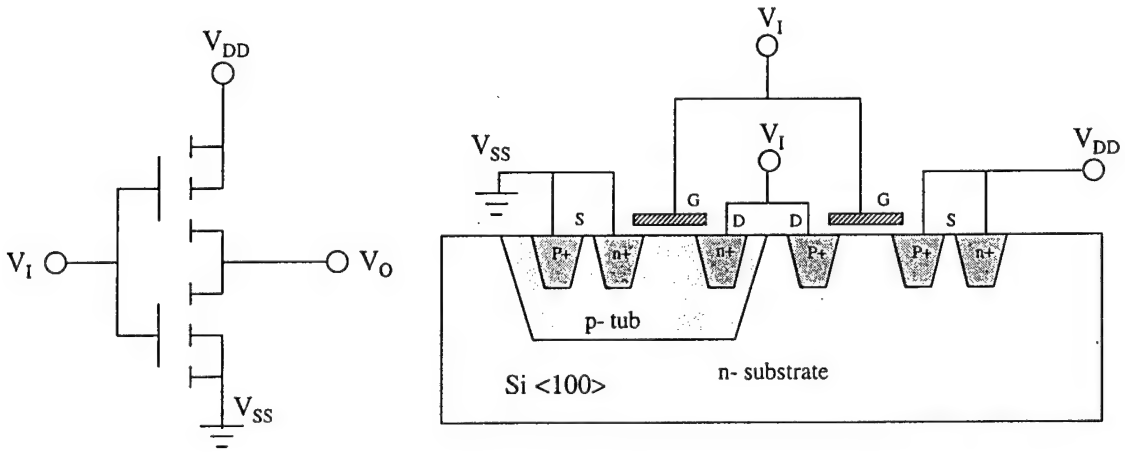


Figure 9. CMOS Inverter.

Equipment, used for our CMOS processing, includes horizontal diffusion furnaces, mask aligners, DC and RF sputtering systems, spin coaters, an RCA clean station, a rinse and dryer, a pattern generator, a stepper, inductively coupled plasma system (ICP), reactive ion etchers, plasma enhanced chemical vapor depositors, evaporators, measurement equipment, and a variety of design software packages.

ICP produces high plasma densities at low pressure with exceptional uniformity resulting in controlled deep anisotropic etching to buried oxide layers. The absence of undercutting at the oxide interface is one of the exceptional features of this process.

Our baseline CMOS process is hosted in a 7,000 sq. ft. class 10-100 cleanroom, together with other III-V processing equipment. Any device-related project can directly benefit from this CMOS process facility. It can be used to integrate the standard CMOS

chip with specially-designed optoelectronic devices or sensing elements, to integrate electronic devices with MEMS, to fabricate customer designed advanced CMOS devices (i.e. high frequency devices on silicon), to provide a test bed for novel interconnection schemes, and to provide necessary support for packaging research.

5.0 Integrated Circuit Fabrication

The ultimate goal of this program is to demonstrate that GaN and CMOS devices can be fabricated on heterogeneous substrates. During this reporting period we have investigated the processes that would allow us to integrate both devices on a common substrate. Table 2 is a list of the process steps in order for CMOS devices along with process temperatures and times. Table 3 shows the same information for GaN devices. Clearly these processes can not be performed serially. We expect to have to work each device process concurrently while always striving to move to lower temperatures on subsequent processes. Table 4 lists a possible process flow for the integrated circuit fabrication.

Process	Temp	Time	Chemistry
RCA Clean	80C	12 min	H2O:HCl:H2O2 @ 6:1:1
Epitaxial Layer Growth	1200C / 1150C	10 min / 44 min	H2 (+ HCl etch) / SiCl4: B2H6
Sacrificial Oxide Growth	1000C	40 min	O2 gas with 2% HCl Flow rate of 1.5 L/min
Nitride Deposition	750C	5 min	Dichlorosilane (SiCl2H2) and ammonia (NH3)
Photolith to define Field Oxide	100C (soft bake after spin) / 120C (hard bake after dev)	45 sec / 2 min	AZP4110 photoresist / AZ: DI developer
Etch Nitride (RIE)	Operating Temp		CF4 gas to Etch SiO2 layer
Strip Field Oxide Photoresist		5 min / 3 min	Warm 300 T Rinse / O2 plasma etcher
Light Field Implant			Ion implantation
Field Oxide Growth	950C	30 min	O2 gas with 2% HCl Flow rate 1.5 L/min
Etch Nitride		10 min	Phosphoric Acid:DI @ 17:3
RCA Clean 2	80C x 2	12 min x 2	H2O:NaOH:H2O2 @ 5:1:1 and @ 6:1:1
Photolithography for the N-Well Implantation	120C (soft bake after spin) / 120 C (hard bake after dev)	45 sec / 2 min	PR / AZ:DI developer
N-well implantation			Ion implantation
Implant Activation Anneal	1100C	10 min	N2
Strip the N-Well Photoresist		5 min / 3 min	Rinse in 300T PR stripper / O2 plasma etcher
Threshold Voltage Adjust Implant			Ion implantation – Boron Gas
RTA Vth Adjustment	1100C	1 min	Anneal in N2 Gas
Wet Etch		60 sec	50% solution of Buffered Oxide Etchant (BOE)
Grow the Gate Oxide	900C	65 min	O2 gas with 2% HCl Flow rate 1.5 L/min
Deposit the Polysilicon	600C	50 min	Silane (SiH4) and Phosphorous
Photolithography to etch the poly	120C (soft bake after spin) / 120 C (hard bake after dev)	45 sec / 2 min	PR / AZ:DI developer
Etch the Polysilicon (RIE)	Operating Temp		CF4 reaction
Remove the Photoresist		5 min / 3 min	300T rinse / O2 plasma

Photolit to cover NMOS	120C (soft bake after spin) / 120 C (hard bake after dev)	45 sec / 2 min	PR / AZ:DI developer
PMOS Light Implant			Ion Implantation - BF2
Remove PR over NMOS		5 min / 3 min	300T rinse / O2 plasma
Photolithography to cover the PMOS	120C (soft bake after spin) / 120 C (hard bake after dev)	45 sec / 2 min	PR / AZ:DI developer
NMOS Light Implant			Ion implantaion - Phos.
Remove PR over PMOS		5 min / 3 min	300T rinse / O2 plasma
LPCVD spacer	800 C	20 min	Oxygen for oxide growth
Photolithography to etch the Spacer	120C (soft bake after spin) / 120 C (hard bake after dev)	45 sec / 2 min	PR / AZ:DI developer
Etch Spacer (RIE)	Operating Temp		CF3 etch
Remove PR over Spacer		5 min / 3 min	300T rinse / O2 plasma
Photoresist to cover NMOS	120C (soft bake after spin) / 120 C (hard bake after dev)	45 sec / 2 min	PR / AZ:DI developer
PMOS Heavy Implant			Ion Implantation - BF2
Remove PR over NMOS		5 min / 3 min	300T rinse / O2 plasma
Photolithography to cover the PMOS	120C (soft bake after spin) / 120 C (hard bake after dev)	45 sec / 2 min	PR / AZ:DI developer
NMOS Heavy Implant			Ion implantation - AsH3
Remove PR over PMOS		5 min / 3 min	300T rinse / O2 plasma
Anneal the drain and source implants	1000C	1 min	N2 gas
Etch Sacrificial Oxide		15 sec	H2O:HF 10:1
Sputter Titanium	Operating Temp		550 angstroms of Titanium
RTA for Salicide Process	700C	120 sec	Anneal with N2 gas
Wet Etch to remove Titanium		Until Ti is gone	H2O2:H2SO4 1:1
Second Anneal for Ti Silicide Process	1000C	30 sec	Anneal with argon gas
Grow Thin Oxide	1000C	40 min	O2 gas with 2% HCl Flow rate 1.5 L/min
LPCVD Large Cap Oxide	350C	25 min	O2 and SiH4
Polish the cap oxide		Until surface is smooth	H2O:HF 400:1
Photolithography to define the contacts	120C (soft bake after spin) / 120 C (hard bake after dev)	45 sec / 2 min	PR / AZ:DI developer
Reactive Ion Etch for contacts	Operating Temp	40 sec	CF4 reaction flow rate of 9:1 CF4:H2
Remove Photoresist used to define contacts		5 min / 3 min	300T rinse / O2 plasma etcher
Sputter Al		2 min	2um of 98.7% aluminum, 0.8% Si and 0.5% Cu
Metal Layer Polish		Until smooth	Chemical etchant for aluminum
Photolith to define Contacts	120C (soft bake after spin) / 120 C (hard bake after dev)	45 sec / 2 min	PR / AZ:DI developer
Etch Al Metal Layer (RIE)	Operating Temp	2 min	BCl3 chemical etch flow rate of 30 cc/min
Remove PR over Al leads		5 min / 3 min	300T rinse / O2 plasma
Upper Metal Layers			Can repeat last 11 steps

Table 2. CMOS Device Processes.

Process	Temperature	Time	Chemistry
Ni Layer Evap			1000 ang. Ni
Mesa Patterning	Room	1 min	H_2O:AZ351 3.5:1
Mesa Etch	Room	1 min	CH_3COOH: HNO_3 :H_20 1:1:2
Mesa Isolation	Operating	8 min	SiCl4 Plasma
Ohmic Patterning	Room	10 minutes	Chlorobenzene
Ohmic Developing	Room	30 sec	H_2O:AZ351 3.5:1
RIE Scuff			
Clean Wafer	Room	10 sec	NH_4OH:H_2O 1:10
Ohmic Evap			Ti 250 ang Al 2000 ang Ni 400 ang Au 450 ang
Alloy RTP	900C	30 sec	
Gate Patterning	Room	10 min	Chlorobenzene
Gate Developing	Room	45 sec	H_2O:AZ351 3.5:1
Gate Evap			Ni 100 ang Au 3000 ang

Table 3 GaN Device Process Steps.

Process	Temp	Time	Chemistry
SiC and GaN growth on <111>Si	> 1000C	60-120 min	
Sacrificial Oxide Growth on Si	1000C	40 min	O2 gas with 2% HCl Flow rate of 1.5 L/min
Nitride Deposition	750C	5 min	Dichlorosilane (SiCl2H2) and ammonia (NH3)
Photolith to define Field Oxide	100C (soft bake after spin) / 120C (hard bake after dev)	45 sec / 2 min	AZP4110 photoresist / AZ: DI developer
Etch Nitride (RIE)	Operating Temp		CF4 gas to Etch SiO2 layer
Strip Field Oxide Photoresist		5 min / 3 min	Warm 300 T Rinse / O2 plasma etcher
Light Field Implant			Ion implantation
Field Oxide Growth	950C	30 min	O2 gas with 2% HCl Flow rate 1.5 L/min
Etch Nitride		10 min	Phosphoric Acid:DI @ 17:3
RCA 2	80C x 2	12 min x 2	H2O:NaOH:H2O2 @ 5:1:1 and @ 6:1:1
Photolithography for the N-Well Implantation	120C (soft bake after spin) / 120 C (hard bake after dev)	45 sec / 2 min	PR / AZ:DI developer
N-well implantation			Ion implantation
Implant Activation Anneal	1100C	10 min	N2
Strip the N-Well Photoresist		5 min / 3 min	Rinse in 300T PR stripper / O2 plasma etcher
Threshold Voltage Adjust Implant			Ion implantation – Boron Gas

RTA Vth Adjustment	1100C	1 min	Anneal in N2 Gas
Wet Etch		60 sec	50% solution of Buffered Oxide Etchant (BOE)
Grow the Gate Oxide	900C	65 min	O2 gas with 2% HCl Flow rate 1.5 L/min
Deposit the Polysilicon	600C	50 min	Silane (SiH4) and Phosphorous
Photolithography to etch the poly	120C (soft bake after spin) / 120 C (hard bake after dev)	45 sec / 2 min	PR / AZ:DI developer
Etch the Polysilicon (RIE)	Operating Temp		CF4 reaction
Remove the Photoresist		5 min / 3 min	300T rinse / O2 plasma etcher
Photolit to cover NMOS	120C (soft bake after spin) / 120 C (hard bake after dev)	45 sec / 2 min	PR / AZ:DI developer
PMOS Light Implant			Ion Implantation - BF2
Remove Photoresist over NMOS		5 min / 3 min	300T rinse / O2 plasma etcher
Photolithography to cover the PMOS	120C (soft bake after spin) / 120 C (hard bake after dev)	45 sec / 2 min	PR / AZ:DI developer
NMOS Light Implant			Ion implantaion - Phos.
Remove Photoresist over PMOS		5 min / 3 min	300T rinse / O2 plasma etcher
LPCVD spacer	800 C	20 min	Oxygen for oxide growth
Photolithography to etch the Spacer	120C (soft bake after spin) / 120 C (hard bake after dev)	45 sec / 2 min	PR / AZ:DI developer
Etch Spacer (RIE)	Operating Temp		CF3 etch
Remove Photoresist over Spacer		5 min / 3 min	300T rinse / O2 plasma etcher
Photoresist to cover NMOS	120C (soft bake after spin) / 120 C (hard bake after dev)	45 sec / 2 min	PR / AZ:DI developer
PMOS Heavy Implant			Ion Implantation - BF2
Remove Photoresist over NMOS		5 min / 3 min	300T rinse / O2 plasma etcher
Photolithography to cover the PMOS	120C (soft bake after spin) / 120 C (hard bake after dev)	45 sec / 2 min	PR / AZ:DI developer
NMOS Heavy Implant			Ion implantation - AsH3
Remove Photoresist over PMOS		5 min / 3 min	300T rinse / O2 plasma etcher
Anneal the drain and source implants	1000C	1 min	N2 gas
Etch Sacrificial Oxide		15 sec	H2O:HF 10:1
Sputter Titanium	Operating Temp		550 angstroms of Titanium
RTA for Silicide Process	700C	120 sec	Anneal with N2 gas
Wet Etch to remove Titanium		Until Ti is gone	H2O2:H2SO4 1:1
Second Anneal for Ti Silicide Process	1000C	30 sec	Anneal with argon gas
Grow Thin Oxide	1000C	40 min	O2 gas with 2% HCl Flow rate 1.5 L/min
Spin-on Glass Planarizing Layer	500C	2 hours	
Ni Layer Evap			1000 ang. Ni
Mesa Patterning	Room	1 min	H_2O:AZ351

			3.5:1
Mesa Etch	Room	1 min	CH_3COOH: HNO_3 :H_20 1:1:2
Mesa Isolation	Operating	8 min	SiCl4 Plasma
Ohmic Patterning	Room	10 minutes	Chlorobenzene
Ohmic Developing	Room	30 sec	H_2O:AZ351 3.5:1
RIE Scuff			
Clean Wafer	Room	10 sec	NH_4OH:H_2O 1:10
Ohmic Evap			Ti 250 ang Al 2000 ang Ni 400 ang Au 450 ang
Alloy RTP	900C	30 sec	
Gate Patterning	Room	10 min	Chlorobenzene
Gate Developing	Room	45 sec	H_2O:AZ351 3.5:1
Gate Evap			Ni 100 ang Au 3000 ang
LPCVD Large Cap Oxide	350C	25 min	O2 and SiH4
Polish the cap oxide		Until surface is smooth	H2O:HF 400:1
Photolithography to define the contacts	120C (soft bake after spin) / 120 C (hard bake after dev)	45 sec / 2 min	PR / AZ:DI developer
Reactive Ion Etch for contacts	Operating Temp	40 sec	CF4 reaction flow rate of 9:1 CF4:H2
Remove Photoresist used to define contacts		5 min / 3 min	300T rinse / O2 plasma etcher
Photolithography to define Deep Si contacts	120C (soft bake after spin) / 120 C (hard bake after dev)	45 sec / 2 min	PR / AZ:DI developer
ICP	Operating Temp	4 min	CF4
Sputter Al		2 min	2um of 98.7% aluminum, 0.8% Si and 0.5% Cu
Metal Layer Polish		Until smooth	Chemical etchant for aluminum
Photolith to define Contacts	120C (soft bake after spin) / 120 C (hard bake after dev)	45 sec / 2 min	PR / AZ:DI developer
Etch Al Metal Layer (RIE)	Operating Temp	2 min	BCl3 chemical etch flow rate of 30 cc/min
Remove Photoresist over Aluminum leads		5 min / 3 min	300T rinse / O2 plasma etcher
Upper Metal Layers			Can repeat last 11 steps, Starting with Grow Thin Oxide Step to create new metal layers
Si Step		GaN Step	New Integrated Step

Table 4 Integrated Process Steps.

Figure 10 is a conceptual diagram of the integrated circuit fabrication process. SiC and GaN growth is performed followed by implants of the CMOS devices. Silicide contacts to the CMOS devices are formed followed by a planarizing glass deposition layer. Isolation and metallization processes for the GaN HFET are completed next. Final contact and interconnection layers to both devices complete the integrated process.

Airbridge interconnects maybe required to minimize the parasitic capacitance of the microwave devices. GTRI has experience in the design and fabrication of airbridge structures as shown in Figure 11.

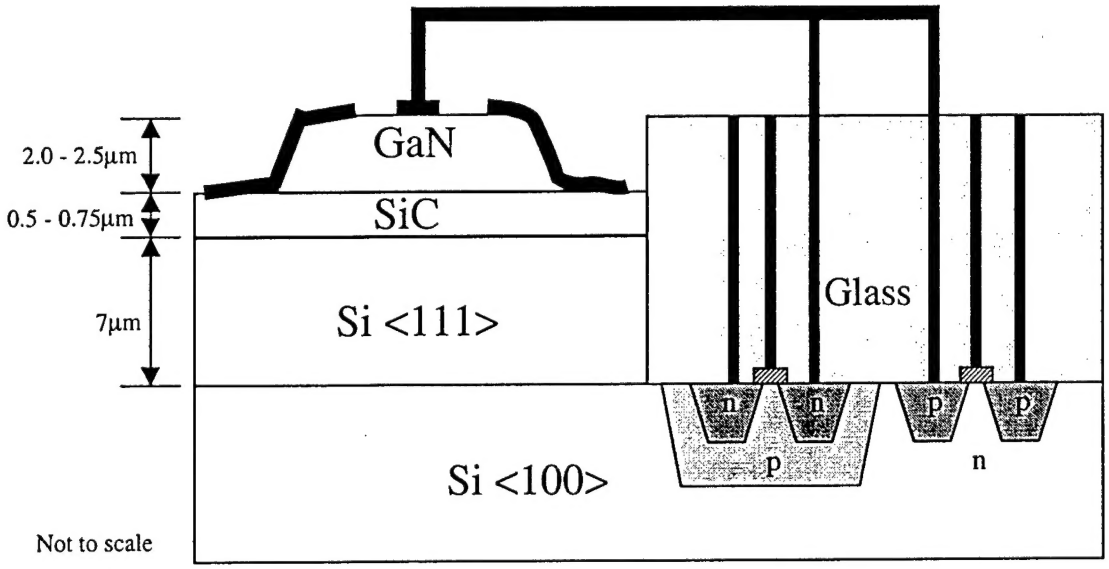


Figure 10. Conceptual Diagram of an Integrated Fabrication Process.

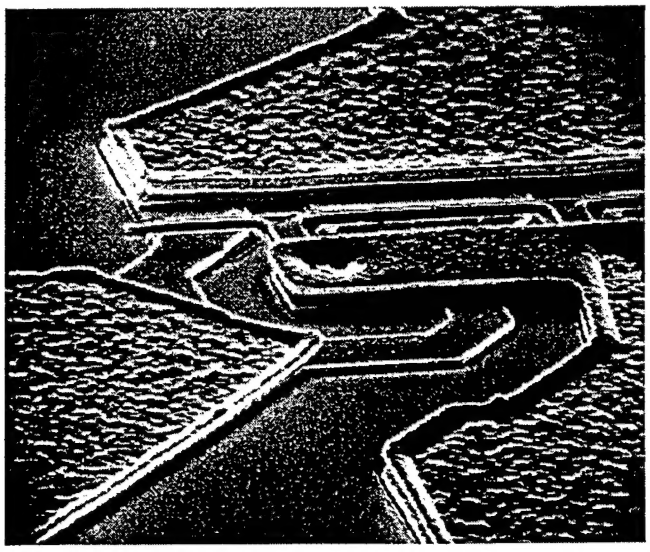
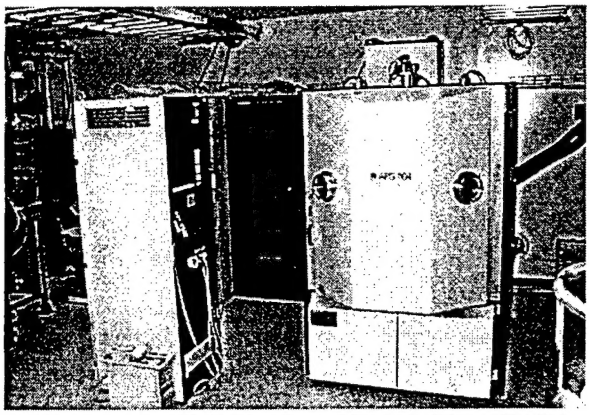


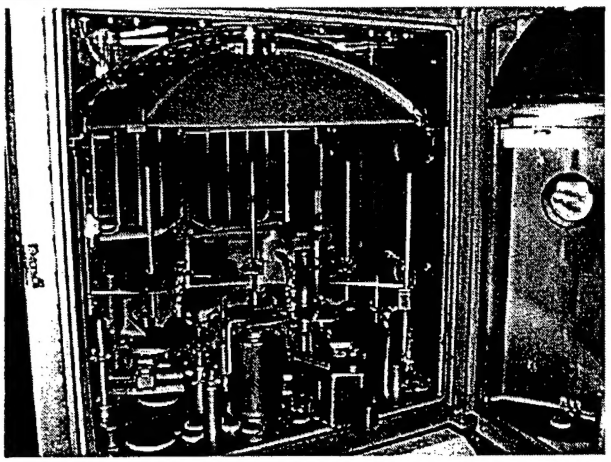
Figure 11. Airbridge Interconnect on a Microwave Transistor.

We will attempt to use the standard fabrication tools as much as practical; however, some processes that normally are performed with a straightforward furnace deposition may have to be accomplished using advanced techniques such as ion assisted deposition (IAD) ahown in Figure 12. The IAD system has a large deposition area/throughput, multi-source evaporation capabilities (thermal and electron beam) and an inert or reactive gas ion assist. It is important to note that the IAD system also excels at the production of high quality dielectric materials and low-temperature deposition of high quality oxide materials. The following is a summary the system's capabilities:

- Large-area flexible manufacturing/research tool
- Four thermal evaporation sources
- One 4-pocket e-beam evaporation source
- Can operate four sources simultaneously
- Individually shuttered sources
- Can control evaporation rates before shutters open
- Substrate temperatures to 400 °C using built-in heater and 600°C using custom-built stationary heater element.
- Uniform low voltage (40-150V), high current density plasma source
- One meter diameter deposition area



Large-area Ion-Assisted Deposition (IAD) System



Inside View of the IAD System

Figure 12. Ion Assisted Deposition System.

ICP will be required to etch the deep trenches necessary to contact the CMOS devices. Figure 13 shows a 350-micron deep trench etched in Si at a rate of 2.8 micron/min. The anisotropy is greater than 0.99.

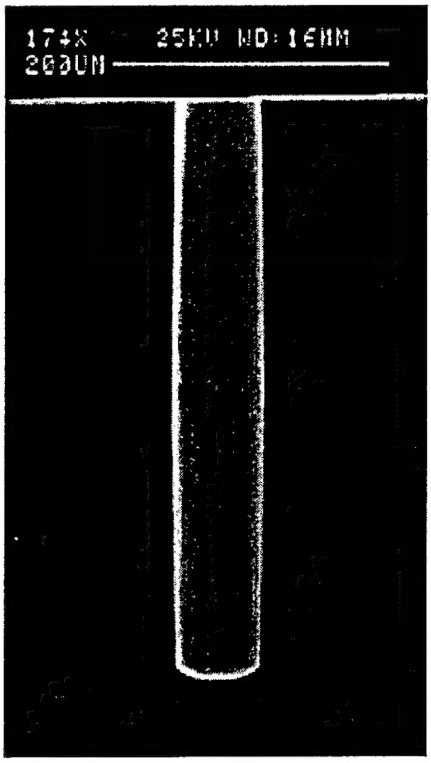


Figure 13. Trench Etching with ICP. (Courtesy of ASE).

6.0 References

[1] S. N. Mohammad, Arnel A. Salvador and Hadis Morkoc, "Emerging Gallium Nitride Based Devices," Proceedings of the IEEE, Vol 83, No. 10, Oct 1995 P 1306-1355.